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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,418	09/30/2003	Yao-Huang Hsieh	MTKP0093USA	2417

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EXAMINER	
VICARY, KEITH E	

ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
07/06/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/605,418	HSIEH, YAO-HUANG	
	Examiner	Art Unit	
	Keith Vicary	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5 are pending in this office action and presented for examination. Claims 1-5 have been amended by amendment filed 6/11/2007.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5 rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamato et al. (Sakamoto) (US 5479342) in view of IBM (IBM Technical Disclosure Bulletin, April 1978, Volume 20, Issue 11B, pages 4877-4878; NB78044877).

4. Consider claim 1, Sakamoto discloses a program counter for storing a program count value (Figure 1, program counter 1); a processing unit coupled to the program counter comprising: (a) an instruction fetching means coupled to the program counter for reading program instructions according to the program count value and storing fetched instructions in a buffer (Figure 1, selector 7, and the logic inherent given the description of Figure 1 in col. 5, lines 48-67, which states that the program counter is transmitted to ROM and RAM and the resulting instruction on the data bus is sent toward the instruction execution unit 5); and (b) an instruction decoding means coupled to the instruction fetching means for decoding and dispatching buffered instructions for execution (Figure 1, instruction executing unit 5; also, col. 5, lines 48-50, which shows

that this unit also decodes); a read only memory coupled to the processing unit for storing a first program (Figure 1, ROM 3); an auxiliary programmable-memory coupled to the processing unit for storing patches to replace corresponding instructions in the first program (Figure 1, RAM 4, shown to store patches in col. 7, line 67, corrected program); and a controller coupled to the program counter and the processing unit for passing an branch instruction corresponding to one of the patches to the processing unit in response to a match between the program count value and an initializing program count value; wherein the processing unit is for executing the indirect branch instruction to thereby insert a replacement program count value corresponding to the match into the program counter (Figure 1, branch instruction generator 8, comparator 6, and col. 5, lines 48-67, compares the content of the program counter and the contents of the memory means and compares them...if the compared data agree with each other...the selector 7 selects the branch instruction generated by the branch instruction generator, which is sent to the instruction execution unit).

However, although Sakamoto supports multiple patches (See Figure 8 for example, multiple comparators), Sakamoto discloses a direct branch instruction instead of an indirect branch instruction, and thus does not disclose an indirect branch instruction, and thus does not disclose a table containing a replacement program count value for each patch.

On the other hand, IBM does disclose of the use of a branch indirect instruction (disclosure text, line 1) and does disclose of a table containing a replacement program

count value for each patch (disclosure text, line 2, branch table 11 of branch addresses).

IBM's teaching of his branch indirect instruction and corresponding table can be used to enter and exit any one of 128 patches from any point in the code of a running system without disturbance or preplanning (IBM, last line of disclosure text).

It would have been readily recognized to one of ordinary skill in the art at the time of the invention that the teaching of IBM fits into the invention of Sakamoto as the teaching of IBM is also aimed at the environment of patches (IBM, last line of disclosure text). Furthermore, it would have been readily recognized to one of ordinary skill in the art at the time of the invention that the indirect branch instruction could replace the direct branch instruction of Sakamoto without rendering the invention of Sakamoto unusable.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of IBM with the invention of Sakamoto in order to enter and exit any one of 128 patches from any point in the code of a running system without disturbance or preplanning (IBM, last line of disclosure text).

5. Consider claim 3, Sakamoto discloses (a) comparing a program count value of a program counter with an initializing program count value (Figure 1, comparator 6; col. 5, lines 50-54, the comparator 6 is supplied with the contents of the program counter 1 and the contents of the register 9 and compares them); (b) inserting a branch instruction with an index into a buffer of an instruction fetching means when a match is made in

step (a) (Figure 1, branch instruction generator 8, comparator 6, and col. 5, lines 48-67, compares the content of the program counter and the contents of the memory means and compares them...if the compared data agree with each other...the selector 7 selects the branch instruction generated by the branch instruction generator, which is sent to the instruction execution unit); (c) executing the indirect branch instruction by a processing unit (Figure 1, branch instruction generator 8, comparator 6, and col. 5, lines 48-67, compares the content of the program counter and the contents of the memory means and compares them...if the compared data agree with each other...the selector 7 selects the branch instruction generated by the branch instruction generator, which is sent to the instruction execution unit); and (d) changing the program count value of the program counter by the processing unit (col. 7, lines 52-56, the address in RAM stores an instruction code; this is also inherent given the execution of the branch instruction).

However, although Sakamoto supports multiple patches (See Figure 8 for example, multiple comparators), Sakamoto discloses a direct branch instruction instead of an indirect branch instruction, and thus does not disclose an indirect branch instruction, and thus does not disclose accessing a table in an auxiliary programmable memory according to the index of the indirect branch instruction.

On the other hand, IBM does disclose of the use of a branch indirect instruction (disclosure text, line 1) and does disclose of a table in another memory containing a replacement program count value for each patch which is indexed (disclosure text, line 2, branch table 11 of branch addresses, index).

IBM's teaching of his branch indirect instruction and corresponding table can be used to enter and exit any one of 128 patches from any point in the code of a running system without disturbance or preplanning (IBM, last line of disclosure text).

It would have been readily recognized to one of ordinary skill in the art at the time of the invention that the teaching of IBM fits into the invention of Sakamoto as the teaching of IBM is also aimed at the environment of patches (IBM, last line of disclosure text). Furthermore, it would have been readily recognized to one of ordinary skill in the art at the time of the invention that the indirect branch instruction could replace the direct branch instruction of Sakamoto without rendering the invention of Sakamoto unusable.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of IBM with the invention of Sakamoto in order to enter and exit any one of 128 patches from any point in the code of a running system without disturbance or preplanning (IBM, last line of disclosure text).

6. Consider claim 2, Sakamoto discloses the controller further comprises: a register for storing the initializing program count value (Figure 1, register 9; col. 5, lines 65-67, the register 9 comprises a 16-bit register for storing a certain address where the execution of the program is to be avoided).

7. Consider claim 4, Sakamoto discloses ending a finished patch program segment with a terminating instruction branch (col. 7, lines 58-61, after the final address of the

corrected program, the instruction executing unit branches off to the address in the ROM).

8. Consider claim 5, Sakamoto discloses the first program is stored in a read only memory (Figure 1, ROM 3), the method further comprising: branching back to the first program in the read only memory with the terminating branch instruction (col. 7, lines 58-61, after the final address of the corrected program, the instruction executing unit branches off to the address in the ROM, and executes the subsequent program).

Response to Arguments

9. Applicant's arguments with respect to claims 1-5 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Picon et al. (US 4751703) discloses of using a branch instruction to branch to patch code.

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Keith Vicary whose telephone number is (571) 270-1314. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

kv

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